



H81H3-I

Rev : A

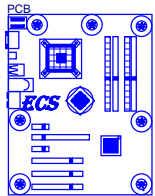
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10	Vcore-RT8889B
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12	F_Panel/FAN/PWR Conn
13	Slot PCI-EX16/miniPCI-EX1
14	HDMI/DVI

REVISION HISTORY:

Page	Index	Rev	Date	Notes
15	PCH-DMI/PE/USB/FDI	VA		Modified from H81H3-M4
16	PCH-DDI/CLK/VGA			
17	PCH-Host/SATA			
18	PCH-MISC			
19	PCH Power/GND			
20	USB			
21	SIO-ITE8772			
22	LAN-RT8111GS/8106E			
23	VT1705CF(Chip)			
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25	Power Delivery			
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ECS
CONFIDENTIAL



PCB : 170 x 170
PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

- NOTE:
- 1. Model Code:
 - 2. Modified from H81H3-M4

Elitegroup Computer Systems

Title

Cover Page

Size

Custom

Document Number

H81H3-I

Rev

1.0

Date:

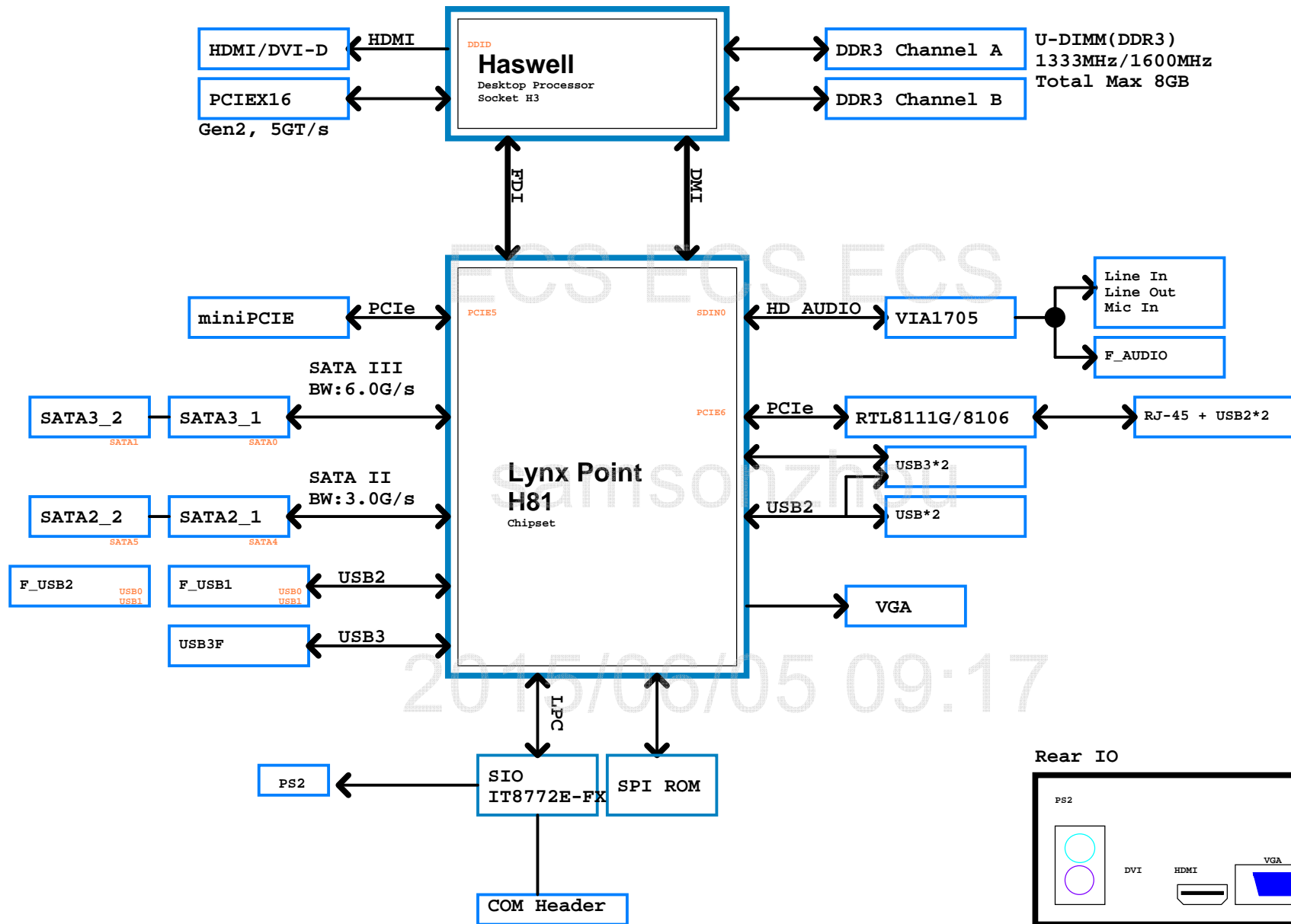
Wednesday, August 14, 2013

Sheet

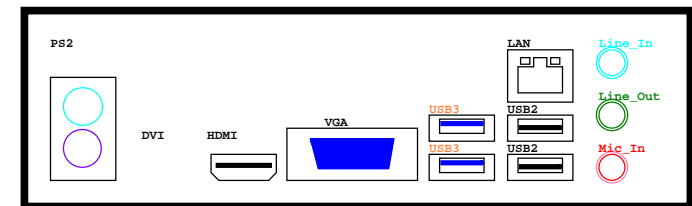
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of

27



Rear IO



Elitegroup Computer Systems

Title			Block Diagram	
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Custom				1.0
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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO0	VCC3	F_Audio Detection	GPI Hi : AC97 ; Lo: HD
GPIO1	VCC3	BOM Selection	GPI Hi : HDMI ; Lo: DVI
GPIO6	VCC3	BOM Selection	GPI
GPIO7	VCC3	BOM Selection	GPI
GPIO13	3VSB	LPC_PME	GPI
GPIO15		DIMM voltage adjust	Hi : 1.35V ; Lo: 1.5V
GPIO24		Me Unlock Control	

SIO-GPIO function

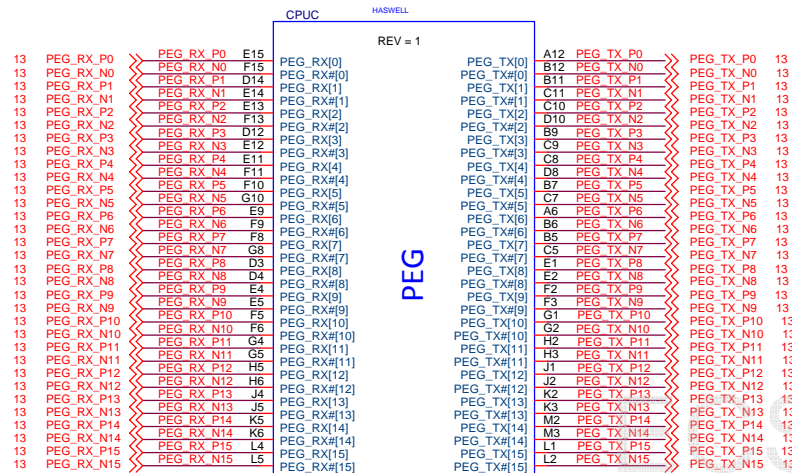
Pin Name	Power Well	Usage	Default Status
GP22	3VSB	G_LED1	GPI
GP23	3VSB	G_LED2	GPI
FAN_TAC2		CPU FAN Tac	
FAN_CTL2		CPU FAN Ctl	
VIN0		Vcore Voltage	
VIN1		Vdimm Voltage	

	S0	S1	S3	S4/S5
GP22	G_LED1	H	H	L
GP23	G_LED2	L	B	L
	G	GB	YB	OFF

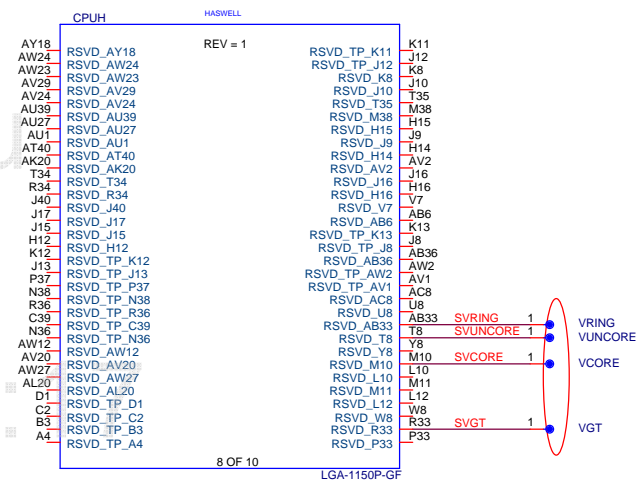
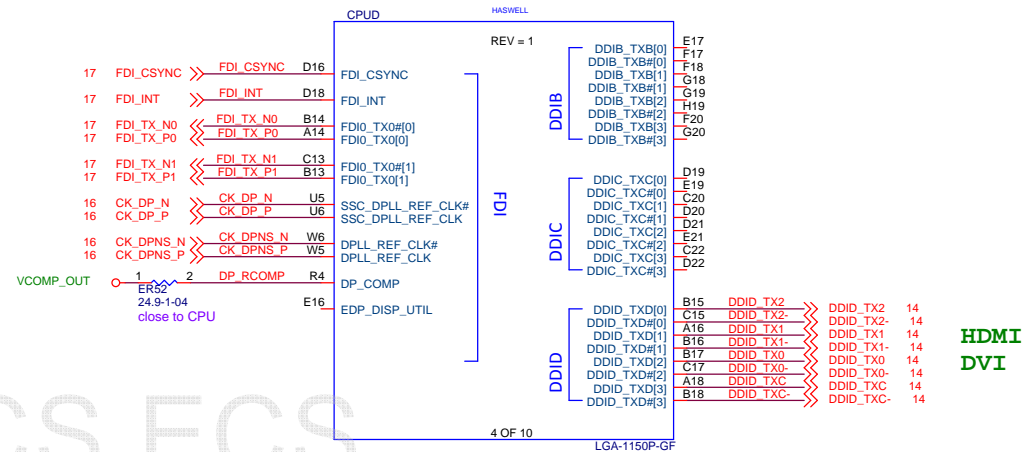
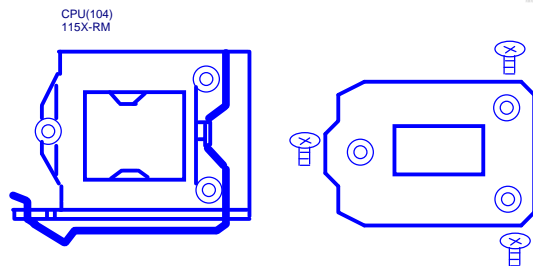
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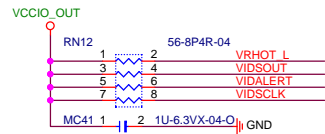
Interrupt mapping

Function	INT# port	PCle*1 port	Device
PCIEX1	INTD#	port 5	LPT integrate
LAN	INTC#	port 6	RTL8111G
SATA	INTB#	NA	LPT integrate

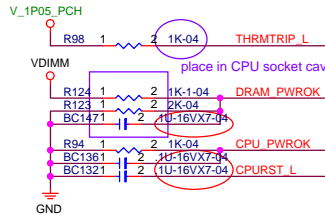


VCOMP_OUT 1 2 PEG_RCOMP P3
 ER44 24.9-1-04
 close to CPU

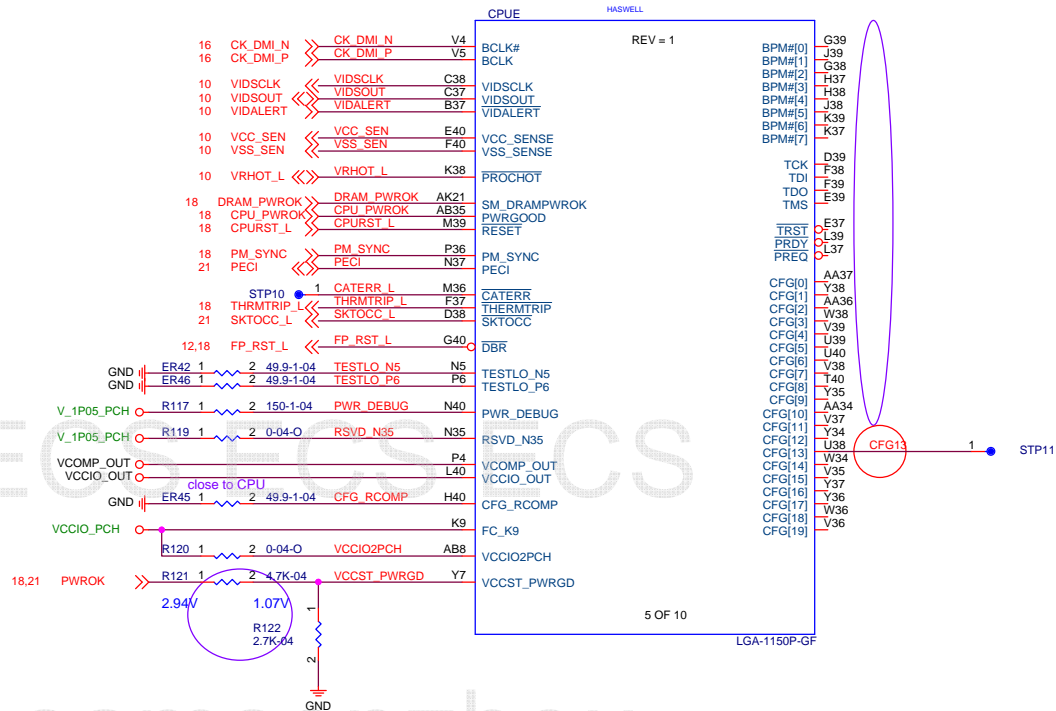
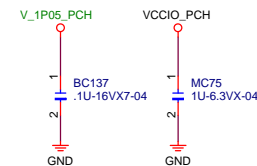




SPEC:
HOT: CPU 51,
SOUT: CPU 110, PWM 110,
ALERT: CPU 75,
CLK: PWM 55,



SPEC: 1V
Origin: Rt: 1.8K 5%, Rb: 3.3K 5%, 0.971V



CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.
CFG[3]: MSR Privacy Bit Feature
1 = Debug capability is determined by
IA32_Debug_Interface_MSR (0xC80) bit[0]
0 = IA32_Debug_Interface_MSR (0xC80) bit[0]
default setting overridden
CFG[5..6]: PCI Express* Bifurcation:
CFG[0..1, 4, 7..19]: Reserved configuration lane.

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	CFG6	CFG5
1 X 16	1	1
2 X 8	1	0
Reserved	0	1
X6 X4 X4	0	0

External Connection

DDR3 CH.A

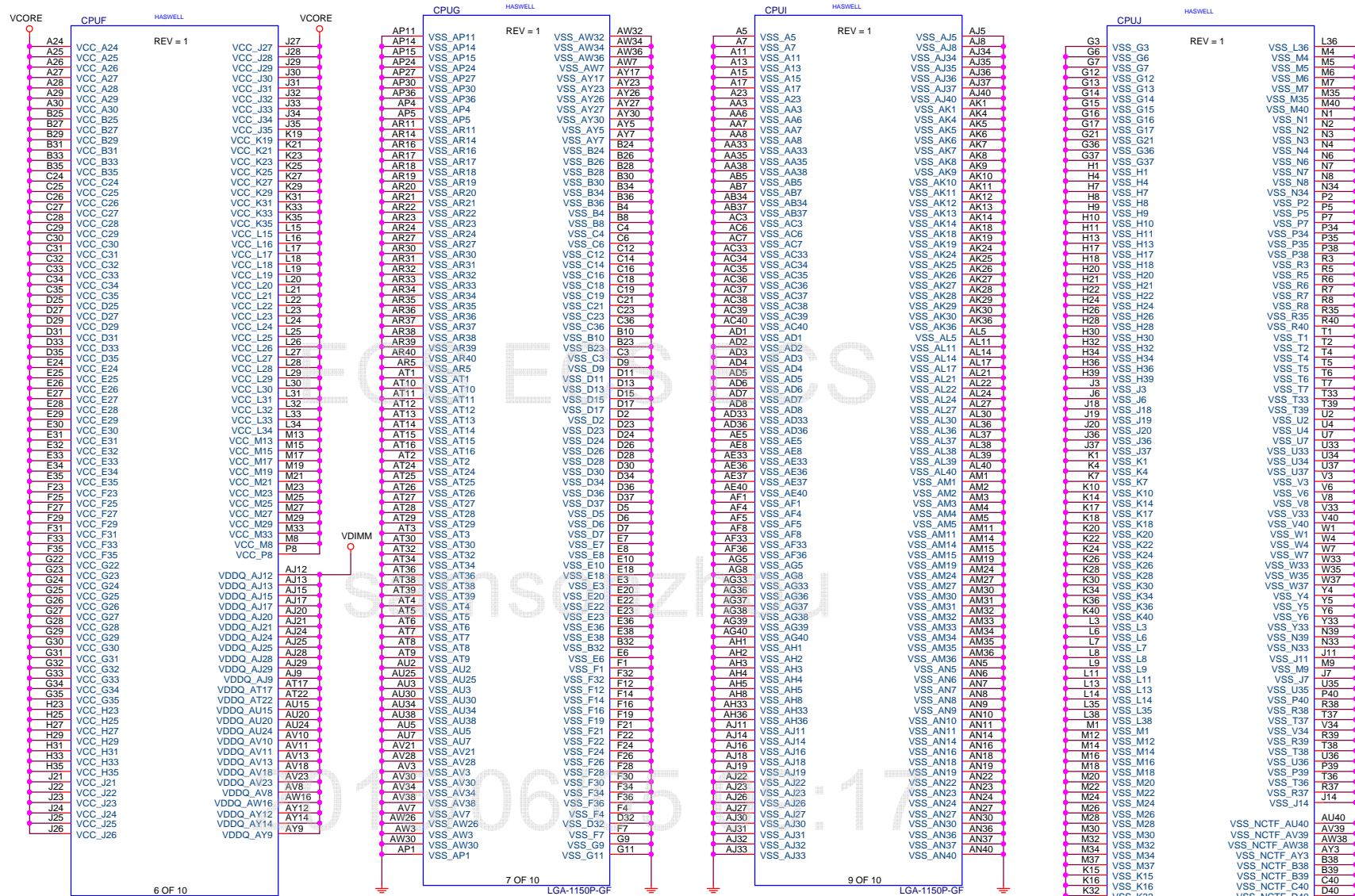
8	M_DATA_A[0..63]	« M DATA A[0..63]
8	M_DQS_A_P[0..7]	« M DQS A P[0..7]
8	M_DQS_A_N[0..7]	« M DQS A N[0..7]
8	M_MA_A[0..15]	« M MA A[0..15]
8	M_BS_A[0..2]	« M BS A[0..2]
8	M_CS_A_L[2..3]	« M CS A L[2..3]
8	M_CKE_A[2..3]	« M CKE A[2..3]
8	M_ODT_A[2..3]	« M ODT A[2..3]
8	M_CLK_A_P[2..3]	« M CLK A P[2..3]
8	M_CLK_A_N[2..3]	« M CLK A N[2..3]
8	DIMM_DQ_A	« DIMM DQ_A
8	M_WE_A_L	« M WE A_L
8	M_CAS_A_L	« M CAS A_L
8	M_RAS_A_L	« M RAS A_L

DDR3 CH.B

9	M_DATA_B[0..63]	« M DATA B[0..63]
9	M_DQS_B_P[0..7]	« M DQS B P[0..7]
9	M_DQS_B_N[0..7]	« M DQS B N[0..7]
9	M_MA_B[0..15]	« M MA B[0..15]
9	M_BS_B[0..2]	« M BS B[0..2]
9	M_CS_B_L[2..3]	« M CS B L[2..3]
9	M_CKE_B[2..3]	« M CKE B[2..3]
9	M_ODT_B[2..3]	« M ODT B[2..3]
9	M_CLK_B_P[2..3]	« M CLK B P[2..3]
9	M_CLK_B_N[2..3]	« M CLK B N[2..3]
9	DIMM_DQ_B	« DIMM DQ_B
9	M_WE_B_L	« M WE B_L
9	M_CAS_B_L	« M CAS B_L
9	M_RAS_B_L	« M RAS B_L
8,9	DRAMRST_L	« DRAMRST_L
8,9	DIMM_CA	« DIMM CA

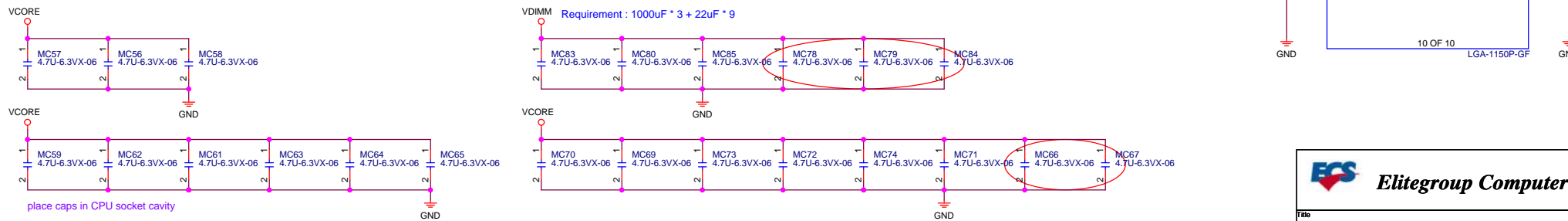
**Attention


		CPUD
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M DATA A1	AD39	SA_DQ[1]
M DATA A2	AF38	SA_DQ[2]
M DATA A3	AF39	SA_DQ[3]
M DATA A4	AD37	SA_DQ[4]
M DATA A5	AD40	SA_DQ[5]
M DATA A6	AF37	SA_DQ[6]
M DATA A7	AF40	SA_DQ[7]
M DATA A8	AH38	SA_DQ[8]
M DATA A9	AH39	SA_DQ[9]
M DATA A10	AK38	SA_DQ[10]
M DATA A11	AK39	SA_DQ[11]
M DATA A12	AH37	SA_DQ[12]
M DATA A13	AH38	SA_DQ[13]
M DATA A14	AK37	SA_DQ[14]
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M DATA A24	AV38	SA_DQ[24]
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M DATA A28	AT37	SA_DQ[28]
M DATA A29	AT38	SA_DQ[29]
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M DATA A37	AV6	SA_DQ[37]
M DATA A38	AW4	SA_DQ[38]
M DATA A39	AY4	SA_DQ[39]
M DATA A40	AR1	SA_DQ[40]
M DATA A41	AR4	SA_DQ[41]
M DATA A42	AN3	SA_DQ[42]
M DATA A43	AN4	SA_DQ[43]
M DATA A44	AR2	SA_DQ[44]
M DATA A45	AR3	SA_DQ[45]
M DATA A46	AN2	SA_DQ[46]
M DATA A47	AN1	SA_DQ[47]
M DATA A48	AL1	SA_DQ[48]
M DATA A49	AL4	SA_DQ[49]
M DATA A50	AJ3	SA_DQ[50]
M DATA A51	AJ4	SA_DQ[51]
M DATA A52	AL2	SA_DQ[52]
M DATA A53	AL3	SA_DQ[53]
M DATA A54	AJ2	SA_DQ[54]
M DATA A55	AJ1	SA_DQ[55]
M DATA A56	AG1	SA_DQ[56]
M DATA A57	AG4	SA_DQ[57]
M DATA A58	AE3	SA_DQ[58]
M DATA A59	AE4	SA_DQ[59]
M DATA A60	AG2	SA_DQ[60]
M DATA A56	AG3	SA_DQ[61]
M DATA A62	AE2	SA_DQ[62]
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M DQS A N2	AN38	SA_DQS[10]
M DQS A N3	AJ36	SA_DQS[11]
M DQS A N4	AW5	SA_DQS[12]
M DQS A N5	AP2	SA_DQS[13]
M DQS A N6	AK2	SA_DQS[14]
M DQS A N7	AF2	SA_DQS[15]
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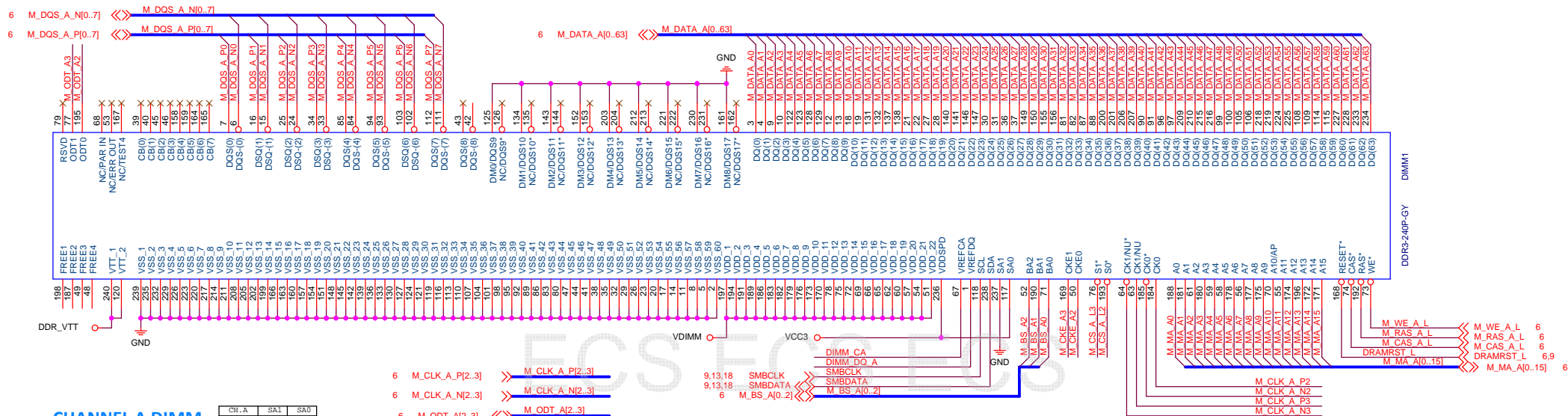
Requirement : 470uF * 5 (+3 no-stuff) + 22uF * 22

Requirement : 1000uF * 3 + 22uF * 9

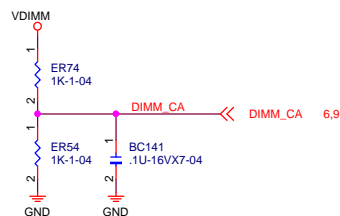


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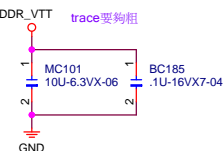
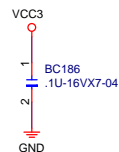
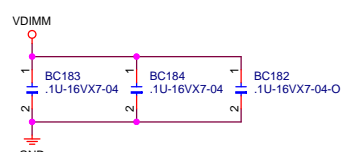
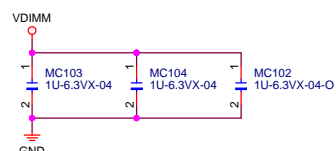
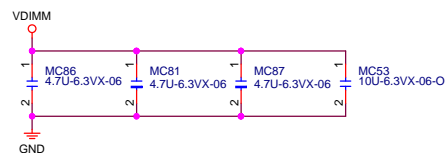
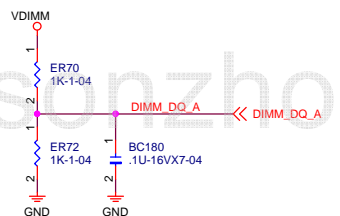
Title			CPU-PWR/GND	
Size	Document Number		H81H3-I	
Customer			Rev 1.0	
Date:	Wednesday, August 14, 2013		Sheet	7 of 27

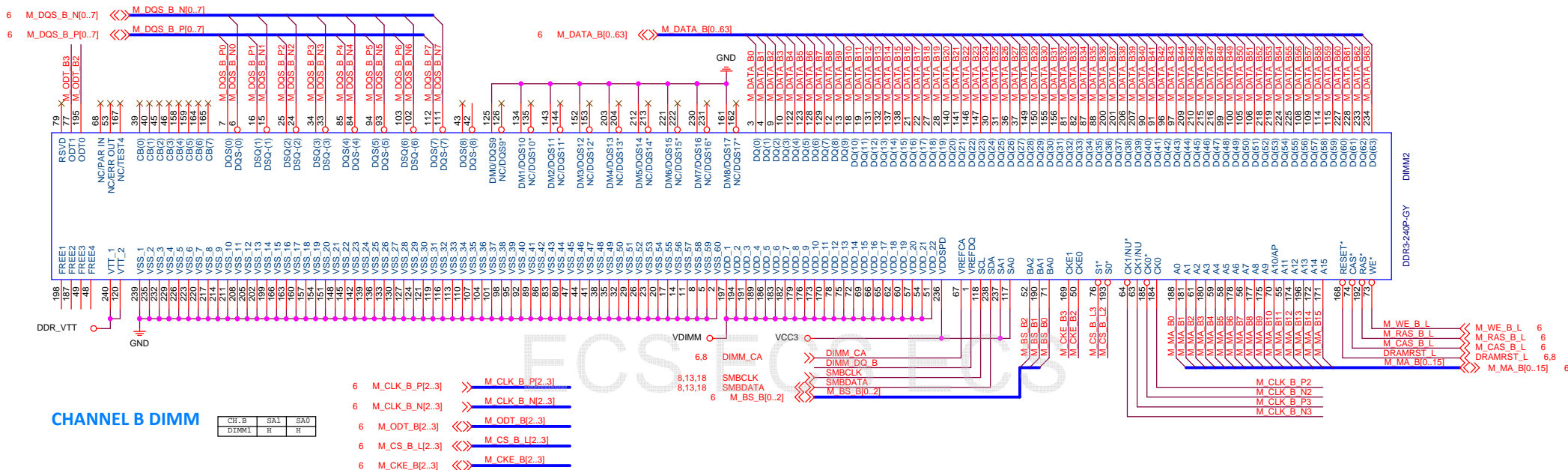


DIMM_VREF_CA Circuit

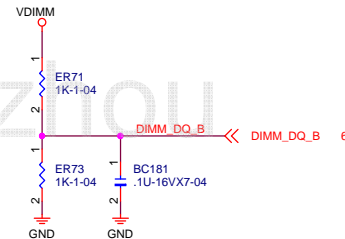


DIMM_VREF_DQ Circuit

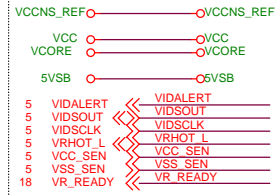




DIMM_VREF_DQ Circuit



External Connection



SET1:

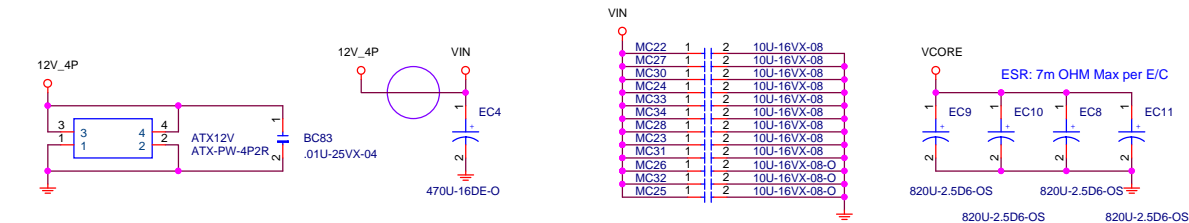
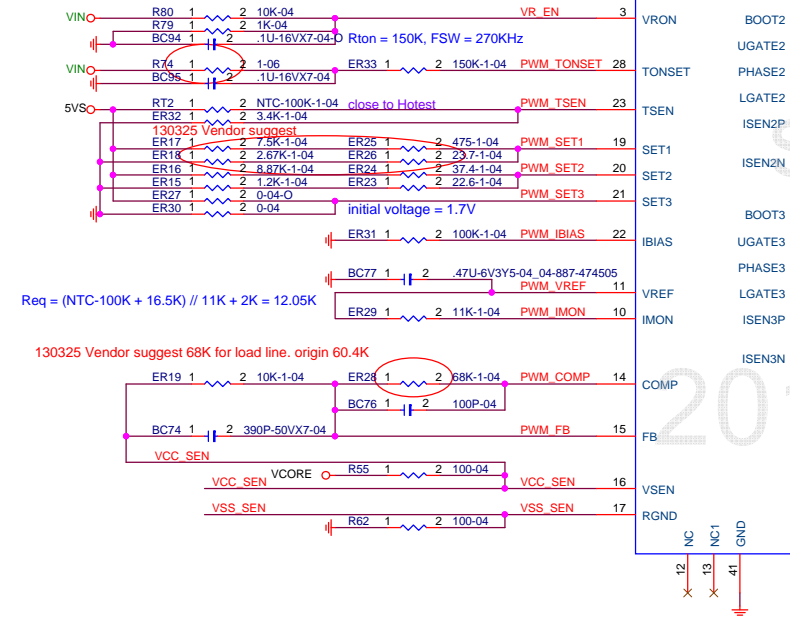
Rt1 = 7.5K+475, Rb1 = 2.67K+23.7,
Ramp (RSET % 130K Rton) = 87.5%, DVID_Width = 192us,
OCP = 150% ICCMAX, DVID_Threshold = 15mV,

SET2:

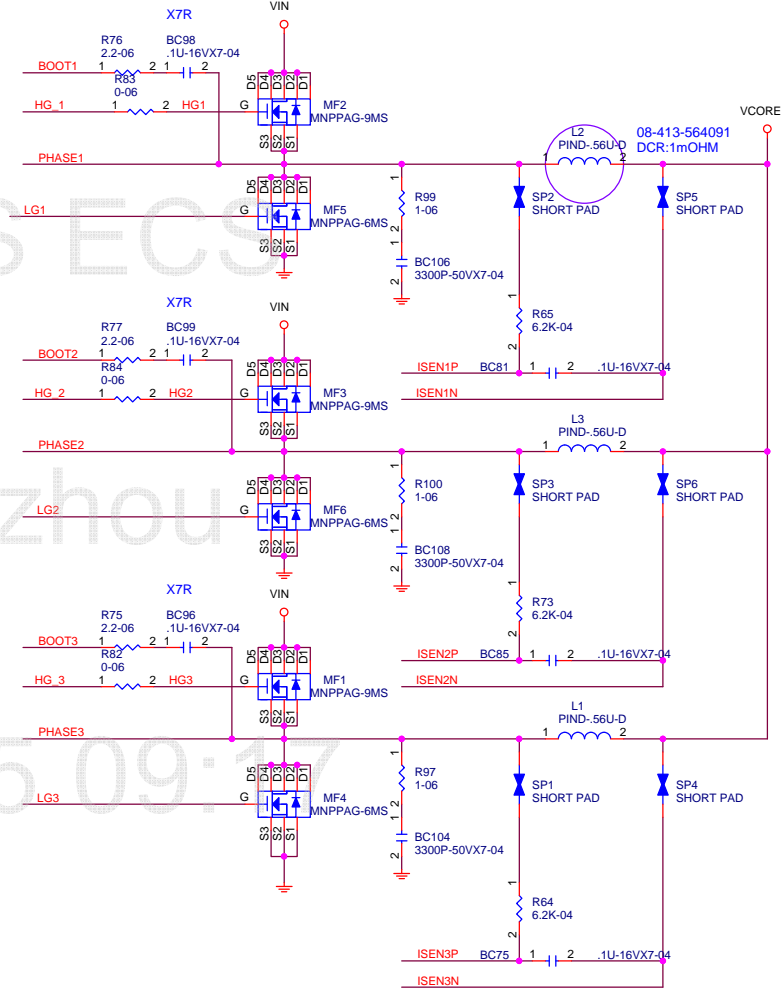
Ri2 = 8.87K+37.4, Rb2 = 1.2K+22.6,
QR Threshold = disable, QR Width = 111%,
ICCMAX = 96A,

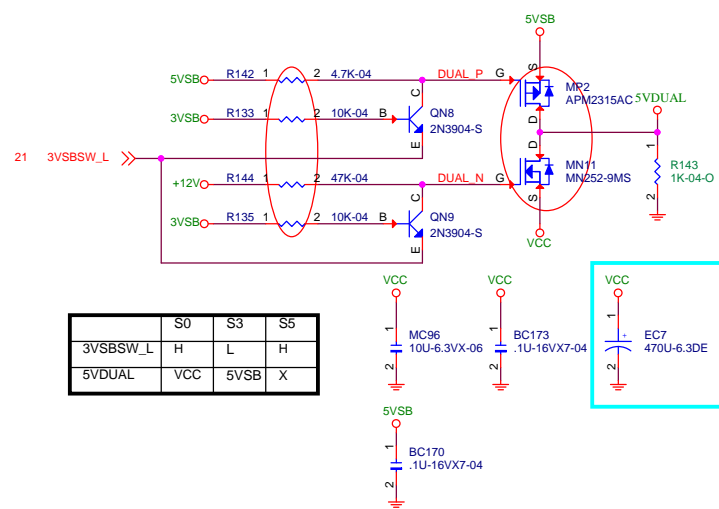
SET3: Rb3 = 0ohm,
Offset = 1/2*(Ri3/Rb3 - 1.2) = 0mV,

When 100u NTC-100K min value : 5.09K,
Visen = 5 * 3.45 / (5.09+3.45) = 1.880 < 1.886,



Power Down Sequencing Circuit



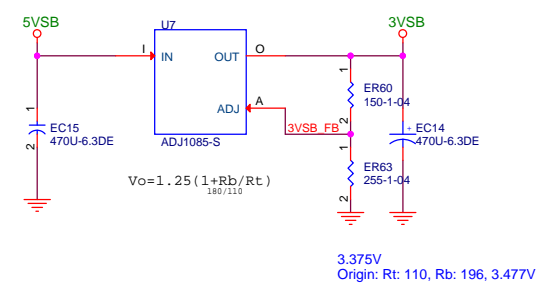
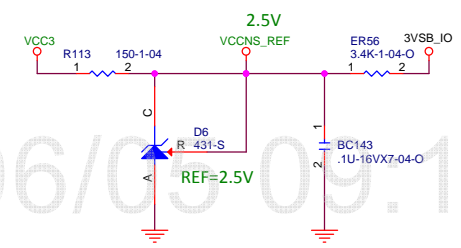
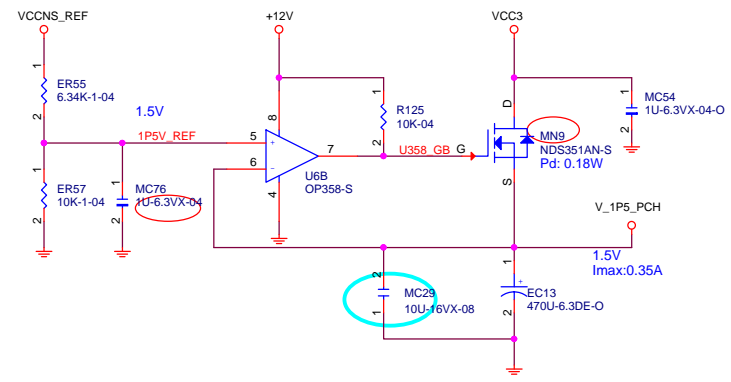


$R_{ocset} = I_{oc} * R_{ds(on)} / 10uA$
 $R_{ocset} = 20K, I_{oc} = 23.53A$
 $4.5+6+5 = 15.5A \text{ max}$

$f = (V_{in} - 0.5) / (3.85p * V_{in} * R_{ton})$
 $R_{ton} = 680K, f = 344K$

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PCH DAC power



Discharge Selection for RT8207M

TON pin connect Rton to	Discharge Mode
Vin	Non-Tracking Discharge

S3 and S5 Truth Table

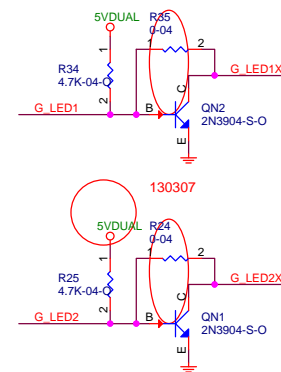
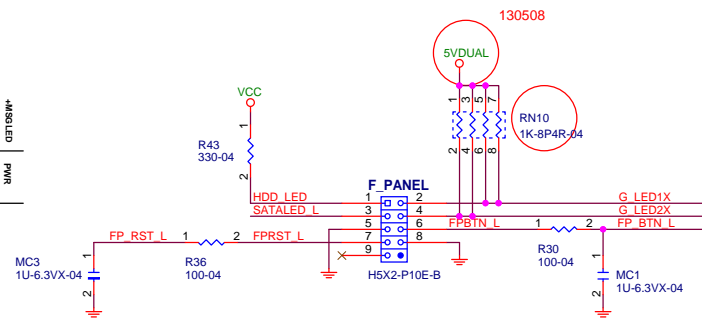
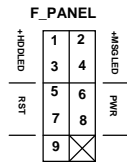
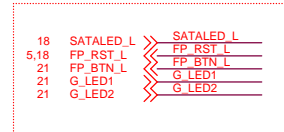
STATE	S0	S3	S5	VDDQ	VTTREF and VTT	VTT
S0	H	H	H	OUTPUT	OUTPUT	OUTPUT
S3	L	H	H	OUTPUT	OUTPUT	HIGH-Z
S4 / S5	L	L	L	DISCHARGE	DISCHARGE	DISCHARGE

FB and output voltage setting

FB	VDDQ(V)	VTTREF and VTT	NOTE
VDD	1.8	Vvddq/2	DDR2
GND	1.5	Vvddq/2	DDR3
FB Resistors	Adjustable	Vvddq/2	0.75V<Vvddq<3.3V

FRONT PANEL

External Connection



GP22	S0	S1	S3	S4/S5
G_LED1	L	B	L	L
G_LED2	L	B	L	L

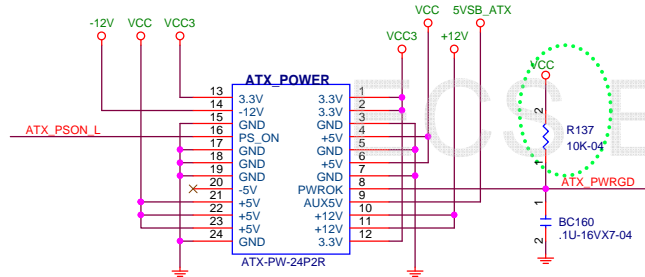
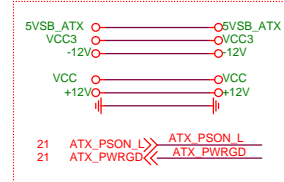
Blinking

GP22	S0	S1	S3	S4/S5
G_LED1	R	H	L	L
G_LED2	L	B	L	L

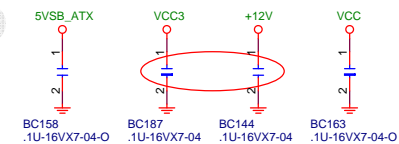
Blinking

POWER CONNECTOR

External Connection



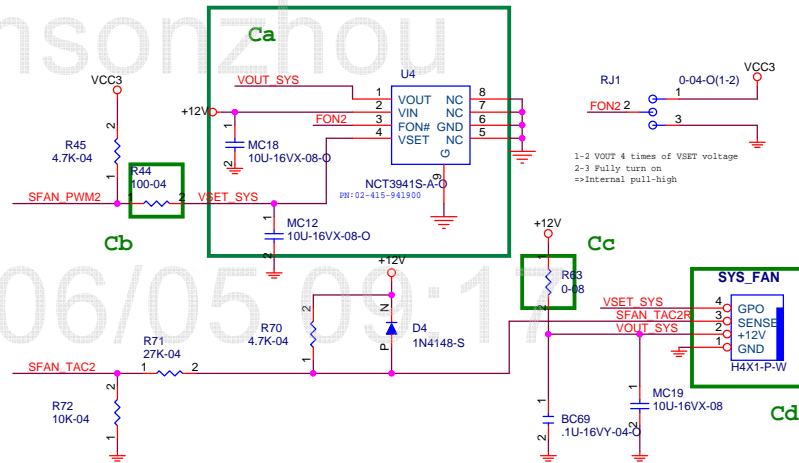
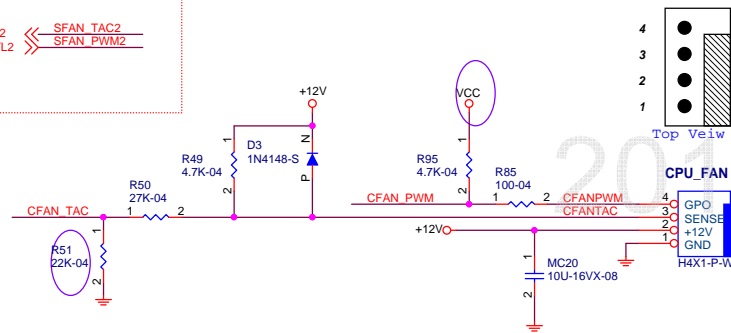
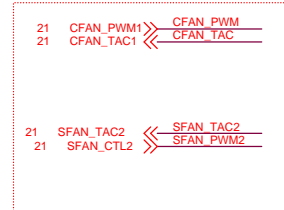
130307 Del VCC EC



For EMI

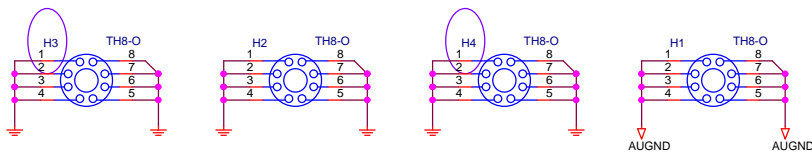
FAN

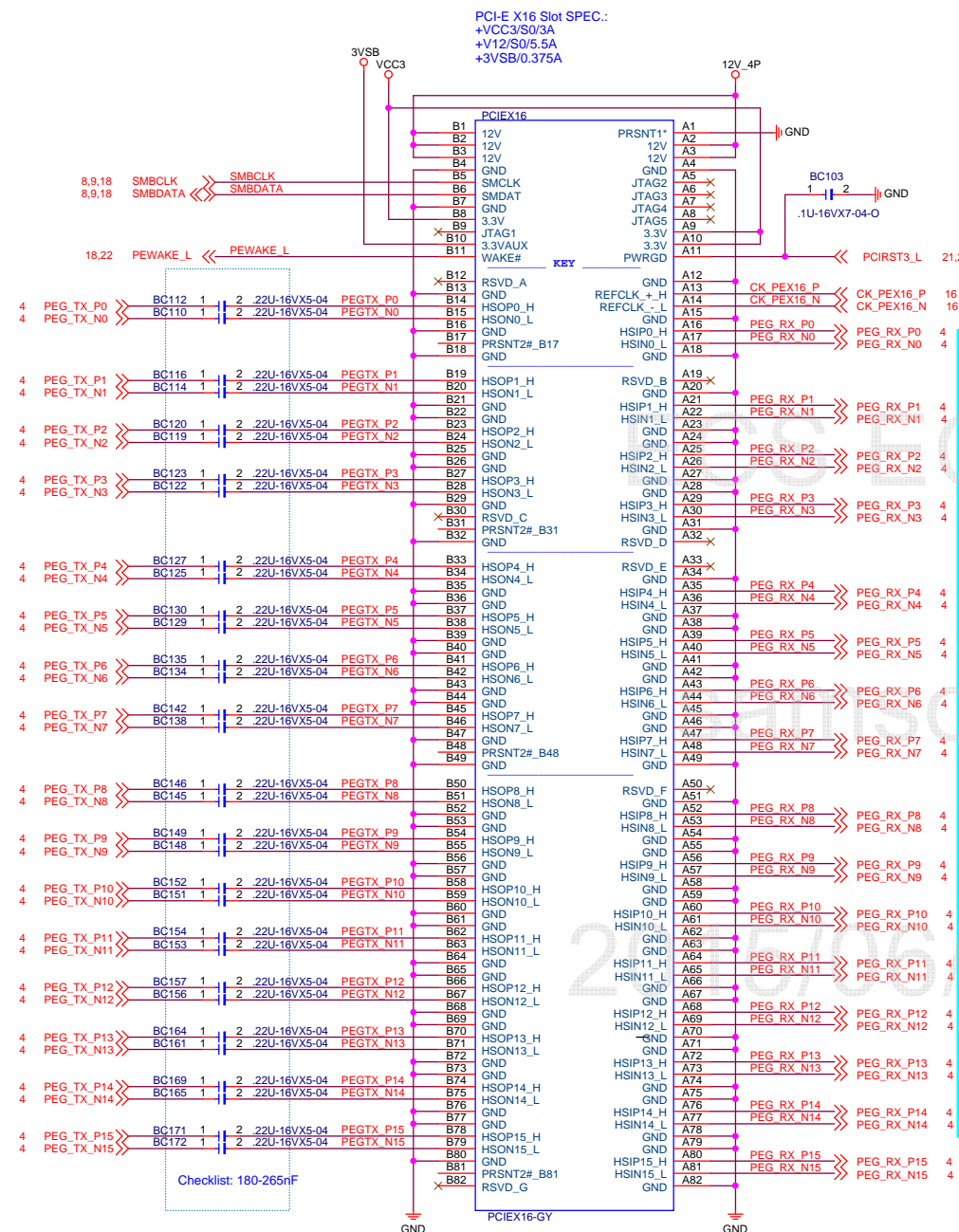
External Connection



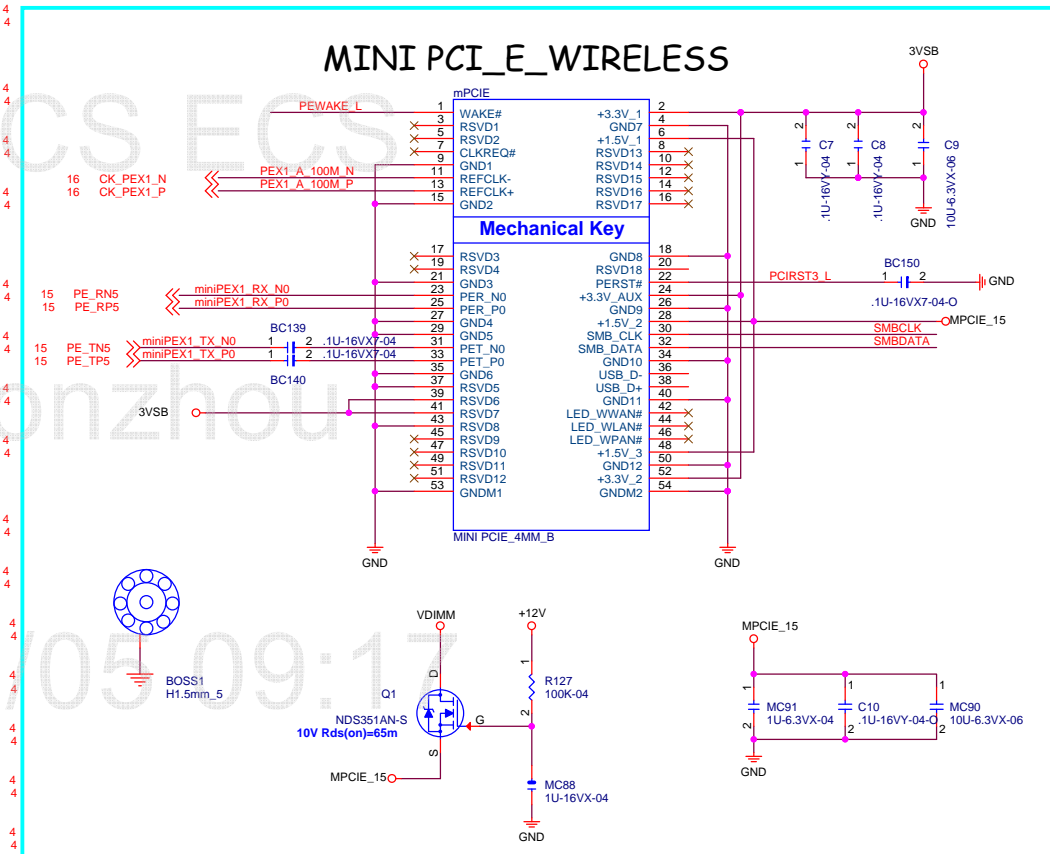
BOM Difference

	SYS_FAN 3PIN	SYS_FAN 4PIN
Ca	V	X
Cb	15k	100
Cc	X	V
Cd	H3X1-P-W	H4X1-P-W





Half-Length PCIe Slot Circuit



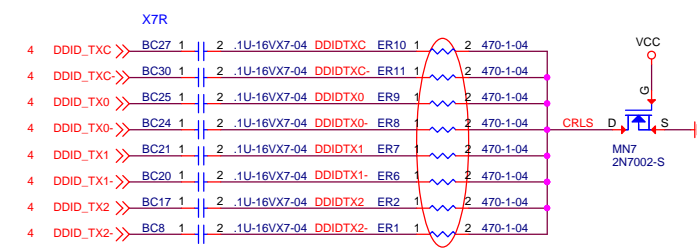
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Slot PCI-EX16 / PCI-EX1

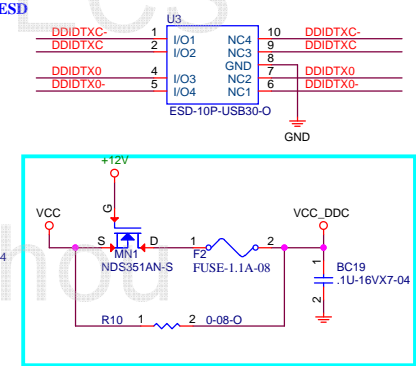
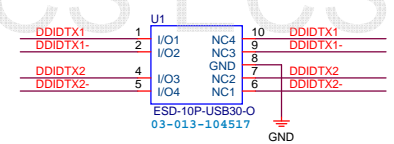
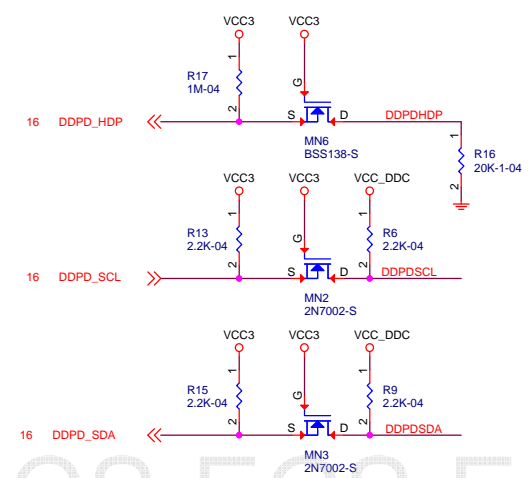
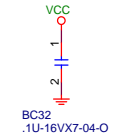
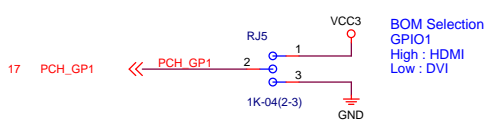
H81H3-I

Rev. 1.0

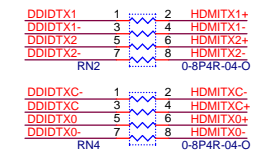
Date: Wednesday, August 14, 2013 Sheet 13 of 27



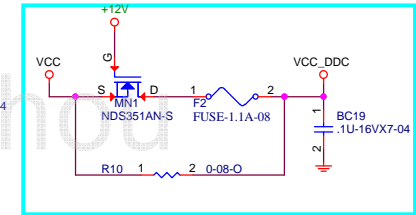
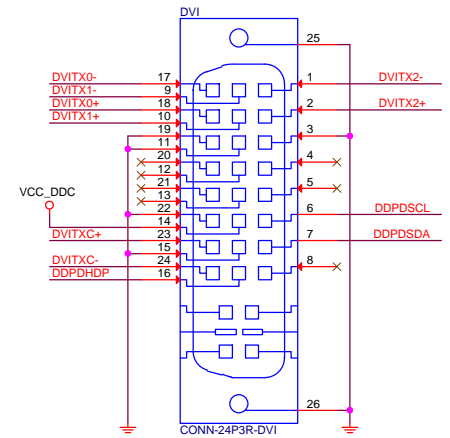
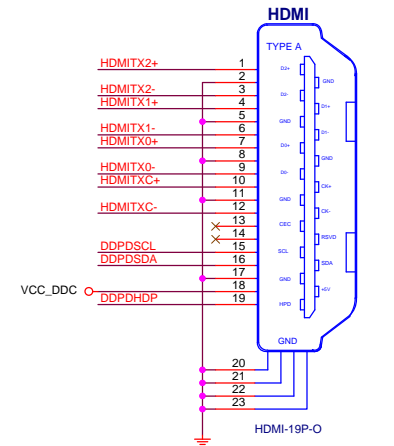
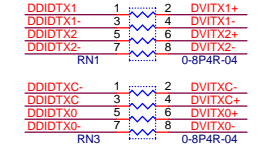
130226 vendor suggest



HDMI

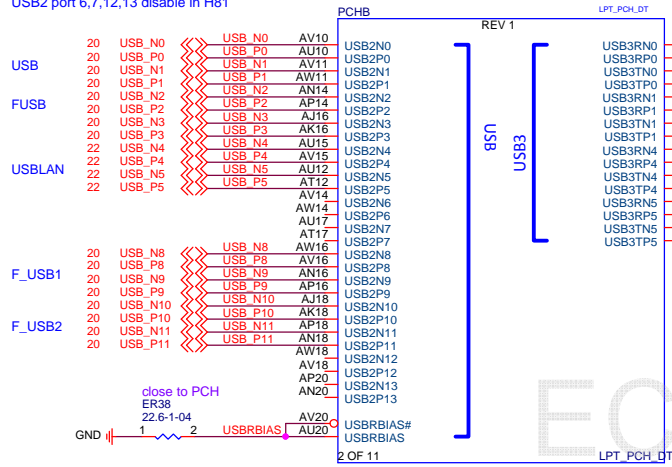


DVI



2015/06/05 09:17

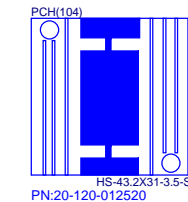
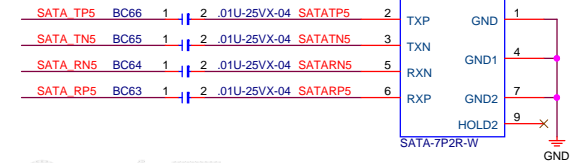
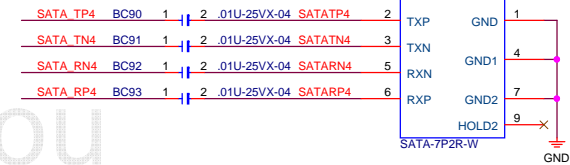
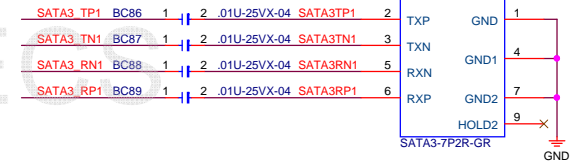
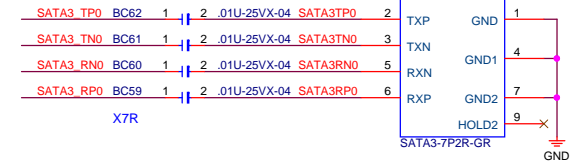
USB2 port 6,7 disable in B85
USB2 port 6,7,12,13 disable in H81



USB3 (PET port 1,2) disable in B85/H81
USB3 port 4,5 disable in H81

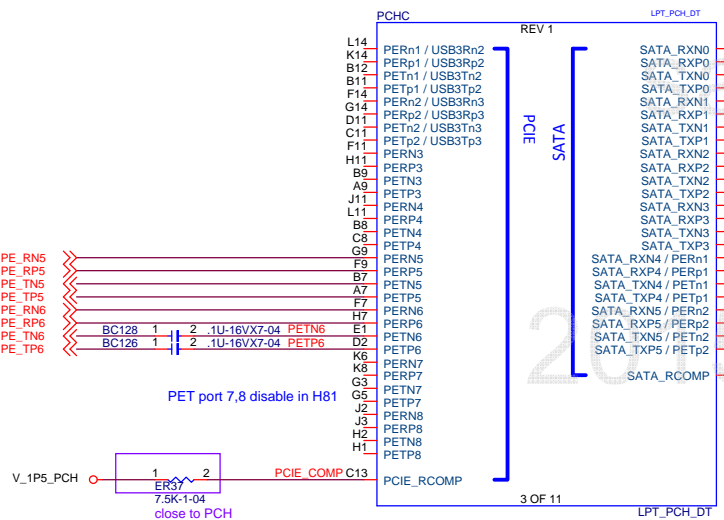
REAR USB3

SATA 6G



PCIEX1

LAN

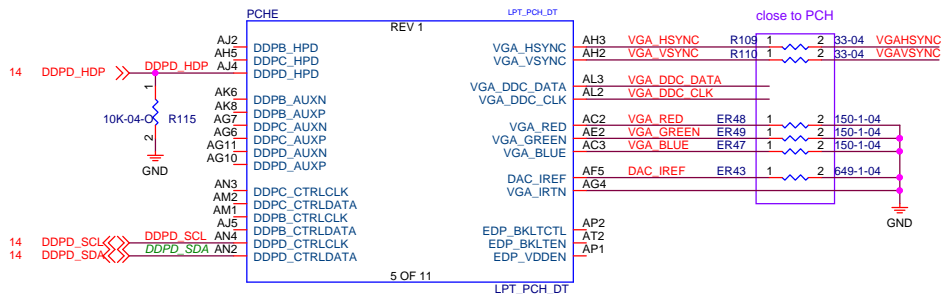


port 2,3 disable in H81
port 4,5 are SATA 3Gb/s in B85/H81

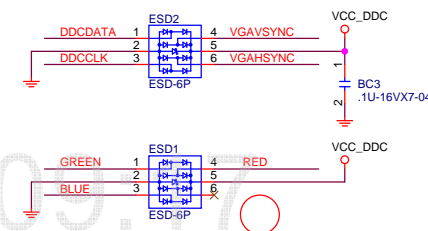
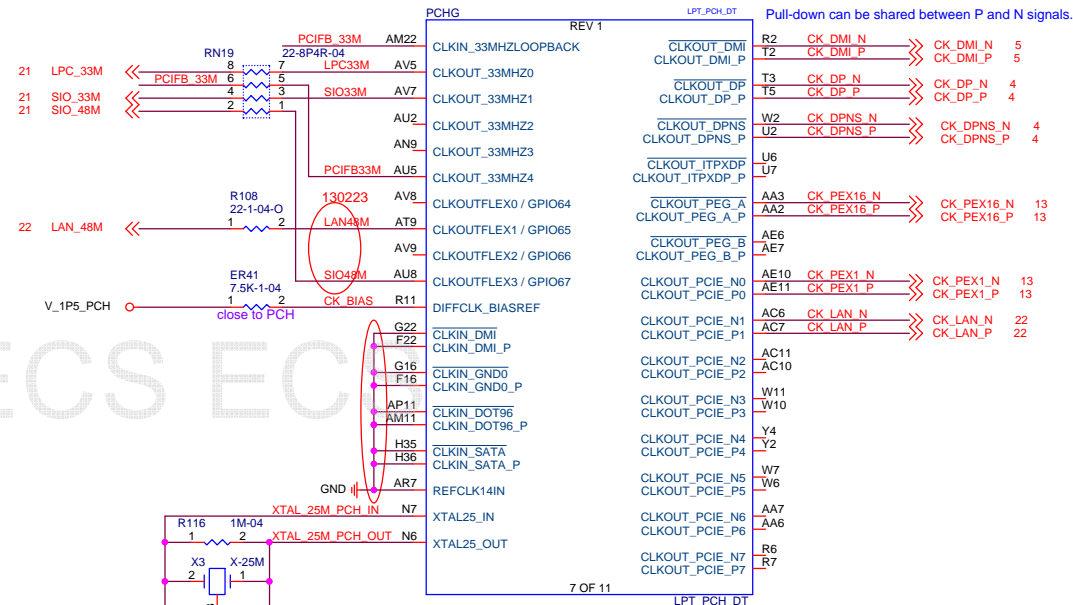
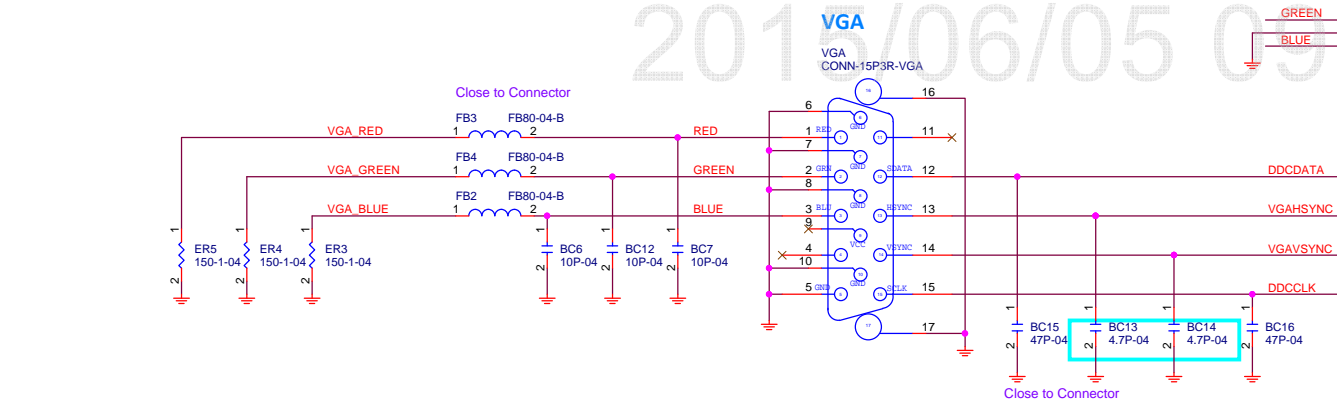
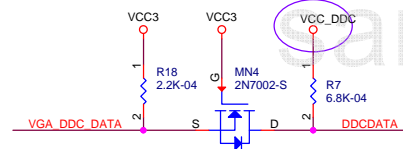
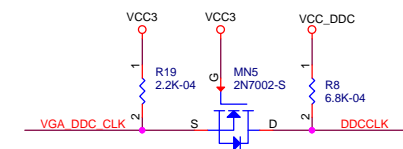
PET port 7,8 disable in H81

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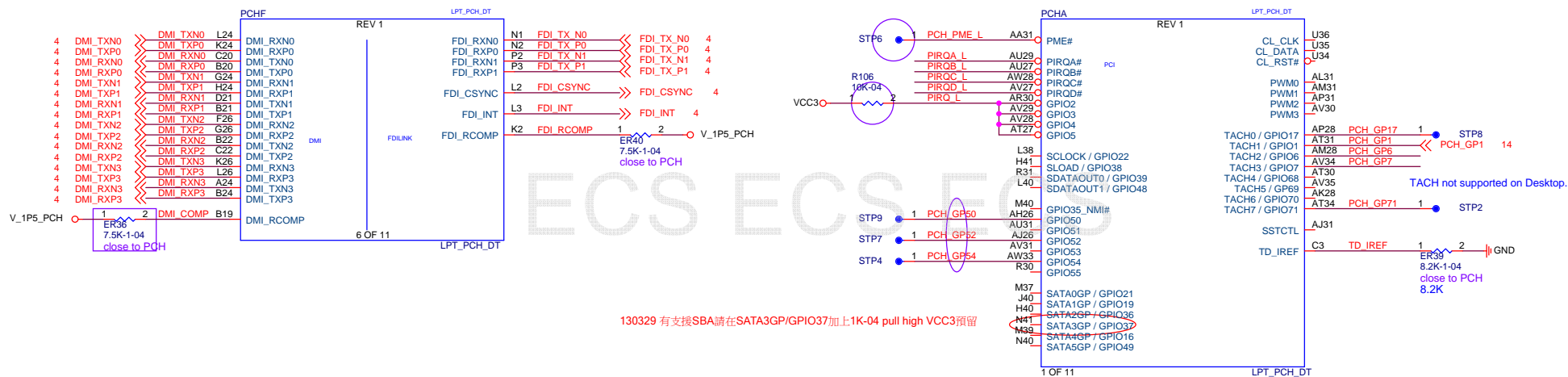
Title		PCH-USB/PE/SATA	
Size	Document Number	H81H3-I	
Custom		Rev	1.0
Date:	Monday, August 19, 2013	Sheet	15 of 27



Port B/C/D Detected
Has a weak internal pull down
0 = is not detected
1 = is detected



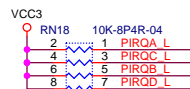
Pull-down can be shared between P and N signals.



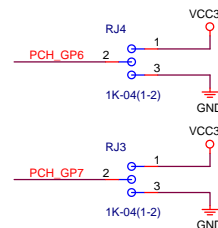
130329 有支援SBA请在SATA3GP/GPIO37加上1K-04 pull high VCC3预留

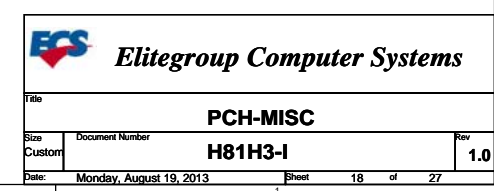
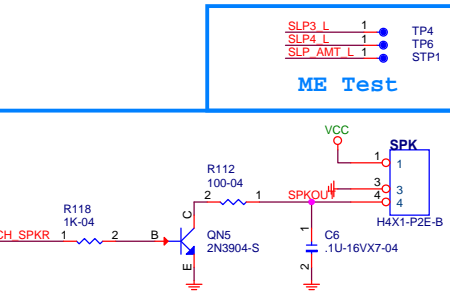
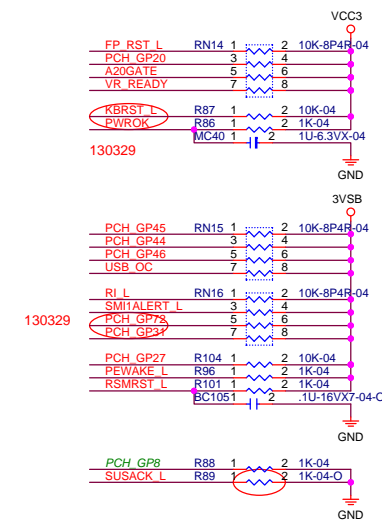
GPIO51,53,55 with 20Kohm internal pull-up
 GPIO53 : DT shouldn't be pulled-down
 GPIO55 : TOP-BLOCK swap override when LOW
 GPIO35,51,53,55 : GPO
 GPIO19 with internal pull-up
 GPIO36,37 with internal pull-down

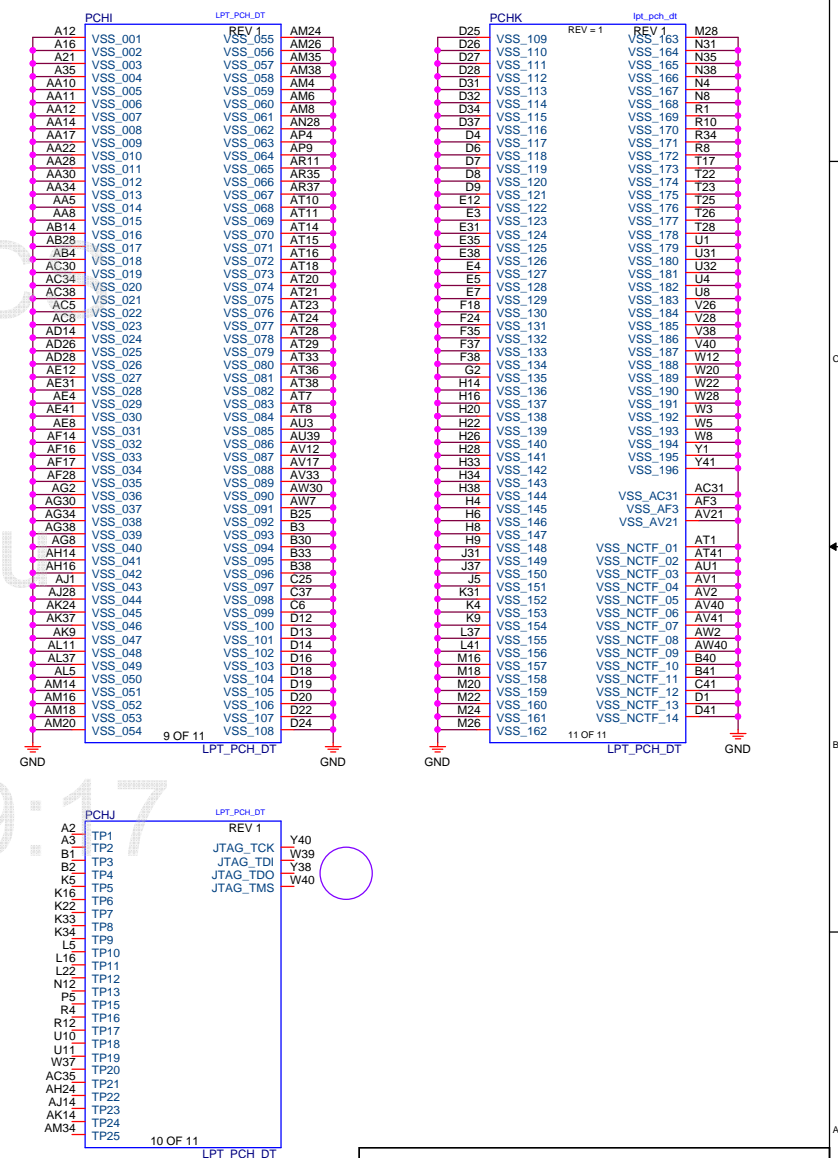
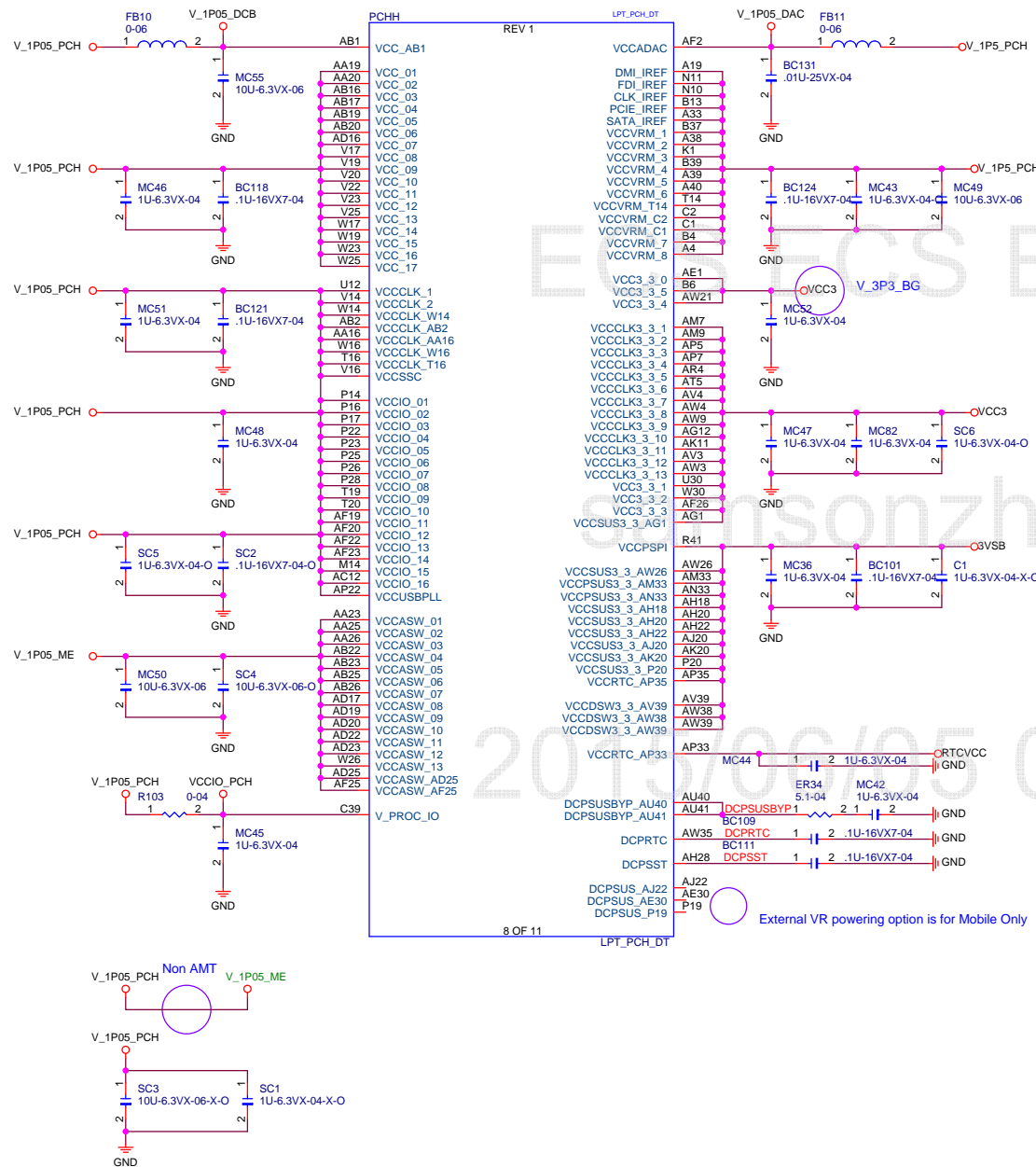
Boot Device	GPIO51	GPIO19
LPC	0	0
SPI	1	1



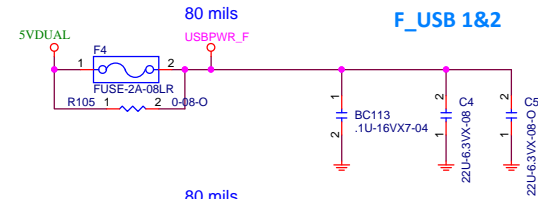
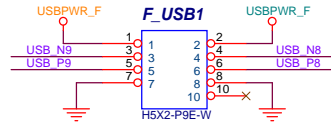
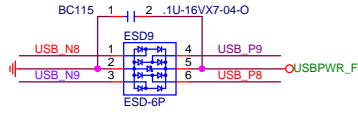
BOM Selection
 *GPIO1(Page14)
 High : HDMI
 Low : DVI
 *GPIO6
 *GPIO7



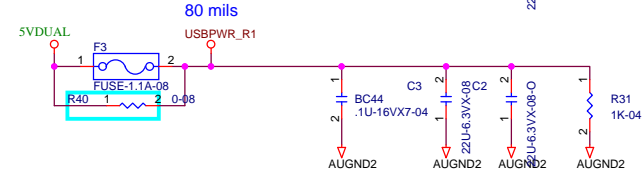
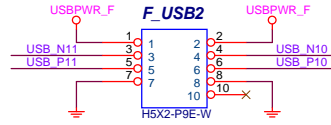
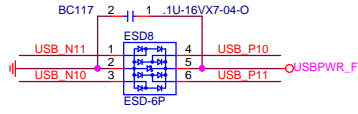




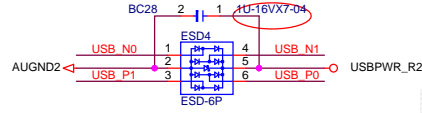
15 USB_P8 <-> USB_P8
15 USB_N8 <-> USB_N8
15 USB_P9 <-> USB_P9
15 USB_N9 <-> USB_N9



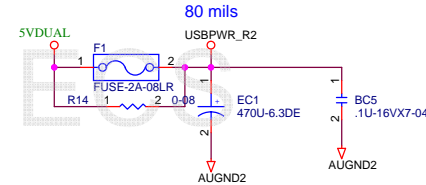
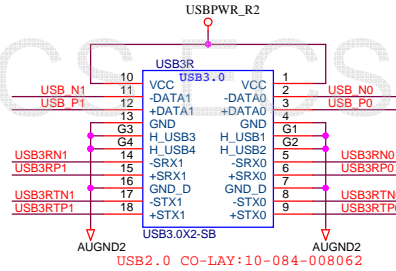
15 USB_P10 <-> USB_P10
15 USB_N10 <-> USB_N10
15 USB_P11 <-> USB_P11
15 USB_N11 <-> USB_N11



15 USB_P0 <-> USB_P0
15 USB_N0 <-> USB_N0
15 USB_P1 <-> USB_P1
15 USB_N1 <-> USB_N1



USB3.0 Connector



15 USB3_TP0 <-> USB3_TP0
15 USB3_TN0 <-> USB3_TN0
15 USB3_RP0 <-> USB3_RP0
15 USB3_RN0 <-> USB3_RN0

USB3_TP0 BC33 1 2 1U-16VX7-04 USB3TP0
USB3_TN0 BC38 1 2 1U-16VX7-04 USB3TN0
USB3_TP1 BC29 1 2 1U-16VX7-04 USB3TP1
USB3_TN1 BC31 1 2 1U-16VX7-04 USB3TN1



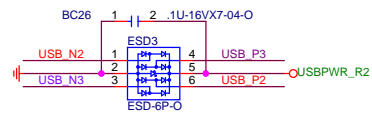
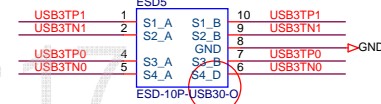
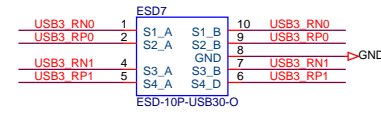
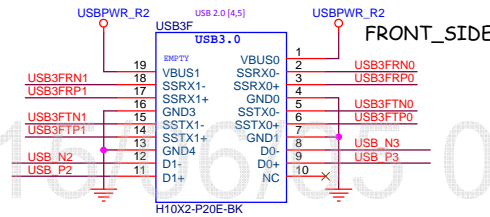
Rear USB3.0



15 USB_N2 <-> USB_P2
15 USB_P2 <-> USB_P2
15 USB_N3 <-> USB_P3
15 USB_P3 <-> USB_P3

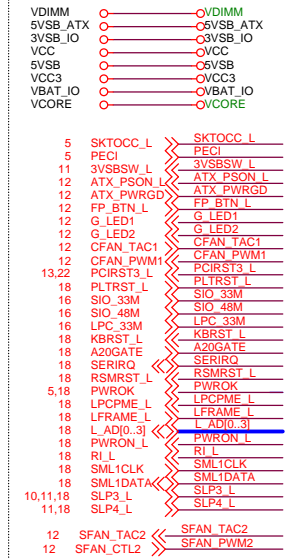


Front USB3.0

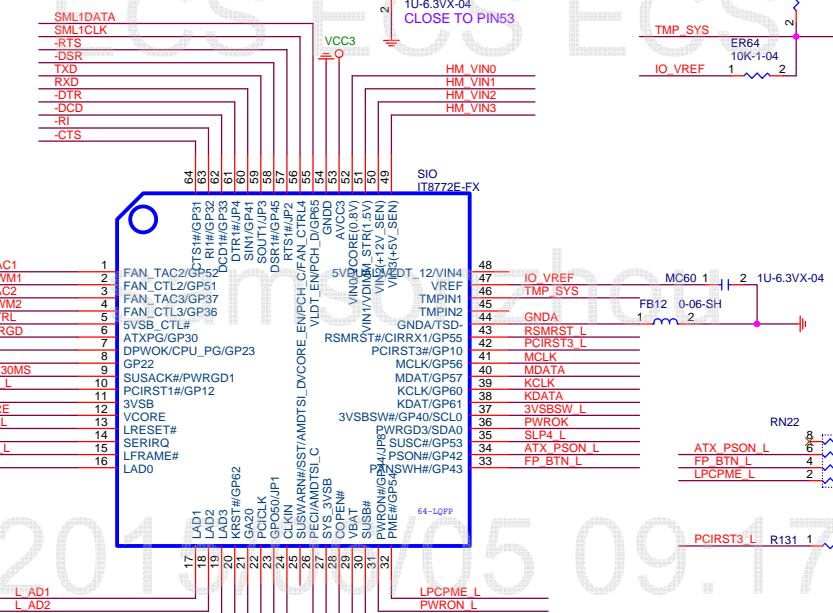
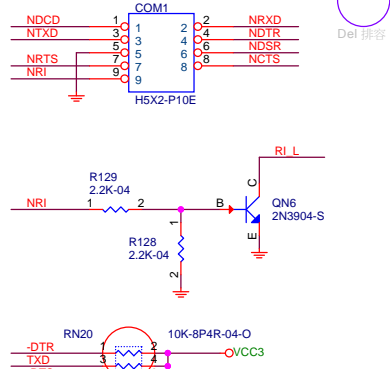


Elitegroup Computer Systems

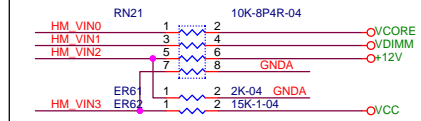
External Connection



COM Header

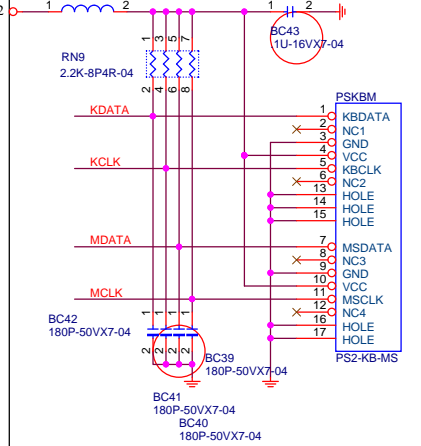


Voltage Monitor

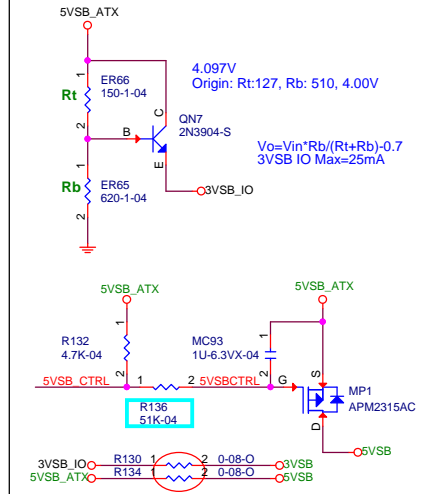


* HM_VIN0 for VCORE
* HM_VIN1 for V_DIMM

PS2



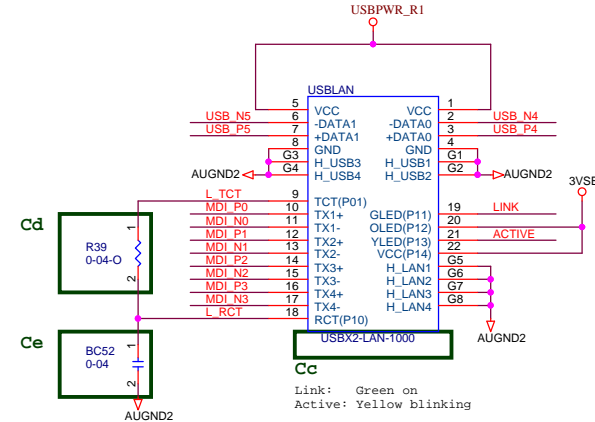
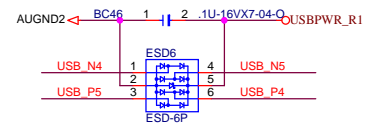
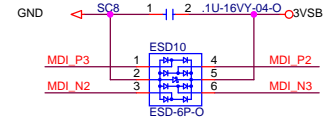
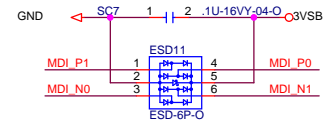
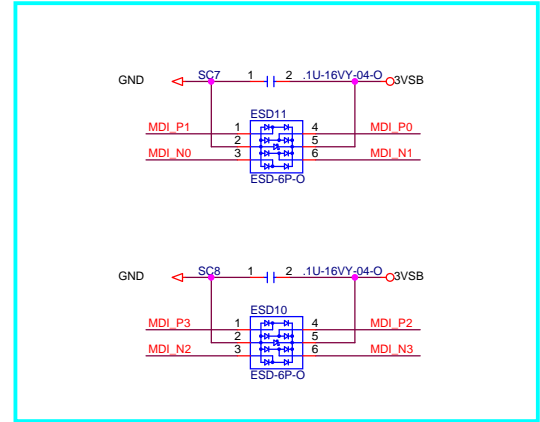
ErP



IT8772 Power-On Strapping Options

Symbol	Value	Description
JP1	DSW_EUP_SEL	1 EUP(default)
Pin-23	WDT_EN	0 Disable WDT to reset PWROK(default)
JP2	WDT_EN	1 Enable WDT to reset PWROK
Pin-57	FAN_CTL_SEL	1 EC Index 6Bh/73h default = 80h
JP3	FAN_CTL_SEL	0 EC Index 6Bh/73h default = 00h
Pin-59	K8PWR_EN	1 Disable K8 Power Sequence(default)
JP4	K8PWR_EN	0 Enable K8 Power Sequence
Pin-61	RSMRST#	1 RSMRST# output detected by 3VSB
JP8	RSMRST#	0 RSMRST# output detected by SYS_3VSB
Pin-31	RSMRST#	0 RSMRST# output detected by SYS_3VSB

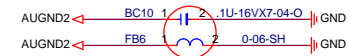
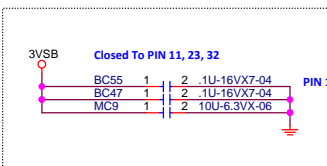
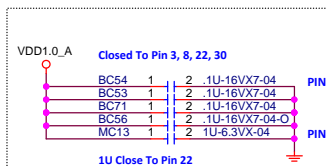
Module Pin	Module Pin Label	USB Module Pin	USB Module Pin Label
3VSB	3VSB	3VSB	3VSB
VCC3	VCC3	VCC3	VCC3
USBPWR_R	USBPWR_R	USBPWR_R1	USBPWR_R1
AUGND2	AUGND2	AUGND2	AUGND2
13,18	PEWAKE_L	PEWAKE_L	PEWAKE_L
13,21	PCIRST3_L	PERSTB	PERSTB
16	CK_LAN_P	CK_LAN_P	CK_LAN_P
16	CK_LAN_N	CK_LAN_N	CK_LAN_N
16	LAN_48M	LAN_48M	LAN_48M
15	PE_TP6	PE_TP6	PE_TP6
15	PE_TN6	PE_TN6	PE_TN6
15	PE_RP6	PE_RP6	PE_RP6
15	PE_RN6	PE_RN6	PE_RN6
15	USB_P4	USB_P4	USB_P4
15	USB_N4	USB_N4	USB_N4
15	USB_P5	USB_P5	USB_P5
15	USB_N5	USB_N5	USB_N5



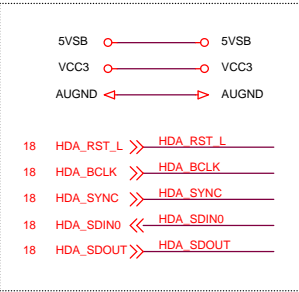
DEFAULT

	RTL8111G-CG (LDO mode) 1000M	RTL8106E-CG (LDO mode) 10/100M
Ca	RTL8111G-CG	RTL8106E-CG
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-25VX-04
Cg	R	X

MC15,BC46,BC35 -O,BC41 1U-6.3VX-04



External Connection



Pin Difference

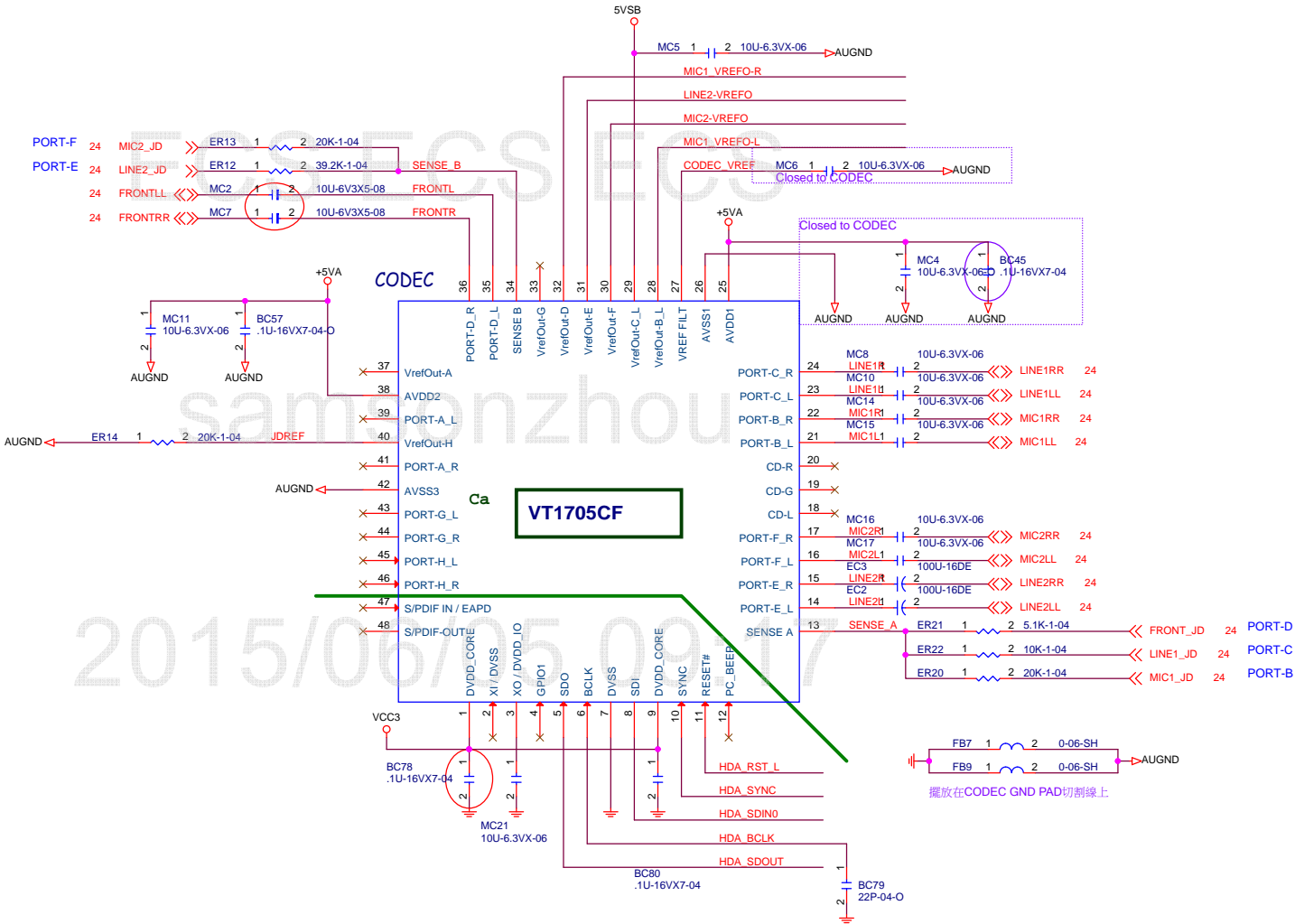
Pin	ALC662VD	VT1705CF
2	GPI00	GPI00/SPDIF_TX1/ DMIC_CLK
3	REG VREF	REGREF
4	GPI01	GPI01/DMIC_DATA
25	LDO OUTPUT	LDO_OUT1
29	LDO VIN	LDO_IN
33	LINE1 VREF	SENSE_C
37	FRONT VREF ?	VREFOUT_C
38	LDO OUTPUT	LDO_OUT2
45	DMIC DATA	NC
46	DMIC CLK	NC
47	EADP	EADP/SPIDF_RX


01-278-662350 02-301-705622

BOM Difference

Location	ALC662VD	VT1705CF
Ca	ALC662-VD0-GR	VT1705CF
Cb	V	X
Cc	2.2K-04	3.3K-04
Cd	75-04	33-04

When you change BOM, remember change GPL to inform BIOS use different VerB-Table.



**Elitegroup Computer Systems**

Title

VT1705CF(Chip)

Size	Document Number	Rev
Custom	H81H3-I	1.0

Date: Wednesday, August 14, 2013

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